MAGNETIC SHIELDING FOR MRAM DEVICES

The Field of the Invention

The present invention generally relates to magnetic random access

5   memory (MRAM) devices, and more particularly to a magnetic random access
memory device having a shield member for shielding the magnetic memory cells
from stray magnetic fields.

Background of the Invention

10   An MRAM device includes an array of memory cells. The typical
magnetic memory cell includes a layer of magnetic film in which the
magnetization is alterable and a layer of magnetic film in which the
magnetization is fixed or "pinned" in a particular direction. The magnetic film
having alterable magnetization may be referred to as a data storage layer or sense

15   layer and the magnetic film which is pinned may be referred to as a reference
layer.

Conductive traces (commonly referred to as word lines and bit lines) are
routed across the array of memory cells. Word lines extend along rows of
memory cells, and bit lines extend along columns of memory cells. Because the

20   word lines and bit lines operate in combination to switch the orientation of
magnetization of the selected memory cell (i.e., to write the memory cell) the
word lines and bit lines can be collectively referred to as write lines.
Additionally, the write lines can also be used to read the logic values stored in
the memory cell.

25   Located at each intersection of a word line and a bit line is a memory
cell. Each memory cell stores a bit of information as an orientation of a
magnetization. The orientation of magnetization of each memory cell will
assume one of two stable orientations at any given time. These two stable
orientations represent logic values of "1" and "0".

30   The orientation of magnetization of a selected memory cell may be
changed by the application of an external magnetic field. The external magnetic

field is created by supplying electrical current to a word line and a bit line which intersect at the selected memory cell. The electrical currents in the word and bit lines create magnetic fields (also referred to as "write fields") surrounding the energized word and bit lines that, when combined, can switch the orientation of

5   magnetization (and thus the logic value) of the selected memory cell. Since no electric power is needed to maintain the memory state of the device, MRAM's are non-volatile.

Preferably, only the selected magnetic memory cell is subjected to both the word and bit line write fields. Other memory cells coupled to the particular

10   word line preferably receive only the word line write field. Other magnetic memory cells coupled to the bit line preferably receive only the bit line write field.

The magnitudes of the word and bit line write fields are usually selected to be high enough so that the chosen magnetic memory cell switches its logic

15   state when subjected to both fields, but low enough so that the other magnetic memory cells which are subject only to a single write field (from either the word line or the bit line) do not switch. The undesirable switching of a magnetic memory cell that receives only one write field is commonly referred to as "half-select" switching.

20   One problem encountered by MRAM devices is the presence of stray or external magnetic fields which emanate from sources other than the word and bit lines which are intended to write to a particular memory cell. Stray magnetic fields can originate from a multitude of sources, both within the MRAM device and external to the MRAM device. In some instances, stray magnetic fields may

25   have a magnitude sufficient to switch the logic state of a memory cell, either as half-select switching or switching in the complete absence of a write field.

The problem of stray fields increases as the storage density of MRAM devices increases. As memory cells are packed closer together, the magnetic fields from adjacent memory cells and their associated write conductors exert a

30   greater effect. Thus, reducing or eliminating the effects of stray magnetic fields becomes more important as storage densities increase.

Summary of the Invention

A magnetic random access memory module comprises a magnetic memory array covered on a first side by a permeable metal layer. An electrically insulating layer is disposed between the permeable metal layer and the magnetic memory array. The permeable metal layer reduces the effects of stray magnetic fields on the magnetic memory array.

Brief Description of the Drawings

Figures 1a and 1b are top and perspective views of a simplified magnetic memory array as known in the prior art.

Figures 2a through 2c illustrate the orientations of magnetization of active and reference magnetic films of a magnetic memory cell like that in Figures 1a and 1b.

Figure 3 is a perspective view of a memory cell like that in Figures 1a and 1b showing the magnetic fields generated by currents flowing through the write lines.

Figure 4 is a cross sectional representation of a memory module according to an embodiment of the invention.

Figures 5a and 5b are perspective and top views of a memory module according to another embodiment of the invention.

Figure 6 is a perspective view of a memory module according to another embodiment of the invention.

Description of the Preferred Embodiments

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following detailed description,

therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

A top plan view of an example of a simplified MRAM array 100 is presented in Figure 1. In Figure 1 and all that follow, it is to be understood that

5   for the sake of clarity the various components of the illustrated devices are not necessarily shown to scale. The MRAM array 100 includes memory cells 120, word lines 130, and bit lines 132. The memory cells 120 are positioned at each intersection of a word line 130 with a bit line 132. Typically, the word lines 130 and bit lines 132 are arranged in orthogonal relation to one another and the

10   memory cells 120 are positioned in between the write lines (130,132), as illustrated in Figure 1b. For example, the bit lines 132 can be positioned above the memory cells 120 and the word lines 130 can be positioned below.

Figures 2a through 2c illustrate the storage of a bit of data in a single memory cell 120. In Figure 2a, the memory cell 120 includes an active magnetic

15   data film 122 (the sense layer) and a pinned magnetic film 124 (the reference layer) which are separated by a dielectric region 126 (the tunnel barrier). The orientation of magnetization in the sense layer 122 is not fixed and can assume two stable orientations is shown by arrow M_1. On the other hand, the pinned reference layer 124 has a fixed orientation of magnetization shown by arrow M_2.

20   The sense layer 122 rotates its orientation of magnetization in response to electrical currents applied to the write lines (130,132) during a write operation to the selected memory cell 120.

The first logic state of the data bit stored in as memory cell 120 is indicated when M_1 and M_2 are parallel to each other as illustrated in Figure 2b.

25   For instance, when M_1 and M_2 are parallel a logic "1" state is stored in the memory cell 120. Conversely, a second logic state is indicated when M_1 and M_2 are anti-parallel to each other as illustrated in Figure 2c. Similarly, when M_1 and M_2 are anti-parallel a logic "0" state is stored in the memory cell 120. In Figures 2b and 2c the dialectic region 126 has been omitted. Although Figures 2a

30   through 2c illustrate the sense layer 122 positioned above the reference layer 124, the reference layer 124 can be positioned above the sense layer 122.

The resistance of the memory cell 120 differs according to the orientations of M_1 and M_2. When M_1 and M_2 are anti-parallel, i.e., the logic "0" state, the resistance of the memory cell 120 is at its highest. On the other hand, the resistance of the memory cell 120 is at its lowest when the orientations of M_1

5   and M_2 are parallel, i.e., the logic "1" state. As a consequence, the logic state of the data bit stored in the memory cell 120 can be determined by measuring its resistance. The resistance of the memory cell 120 is reflected by a magnitude of a sense current 123 (referring to Figure 2a) that flows in response to read voltages applied to the write lines (130,132).

10   The memory cell structure shown in Figure 2a may be referred to as a spin tunneling device in that electrical charge migrates through the tunnel barrier during read operations. This electrical charge migration through the tunnel barrier is due to a phenomenon known as to spin tunneling and occurs when a read voltages is applied to a magnetic memory cell.

15   In Figure 3, the memory cell 120 is positioned between write lines 130,132. For the purpose of clarity, the sense and reference layers 122, 124 are not shown in Figure 3. The orientation of magnetization of the reference layer 122 is rotated in response to a current I_x that generates a magnetic field H_y and a current I_y that generates a magnetic field H_x. The magnetic fields H_x and H_y act

20   in combination to rotate the orientation of magnetization of the sense layer 122 in memory cell 120.

Each memory cell 120 has a switching characteristic for the sense layer 122. That is, a magnetic field having a minimum magnitude equal to H_s is needed to flip the orientation of magnetization of sense layer 122 between its

25   parallel and anti-parallel orientations. In designing an MRAM device, the magnitudes of the H_x and H_y fields are pre-selected so that the resulting field H_w has a magnitude that is greater than or equal to the magnitude H_s needed to write to the magnetic memory cell 120 (that is, to alter the orientation of magnetization of sense layer 122). It may be preferable that the magnitudes of

30   the H_x and H_y fields be slightly larger than necessary to yield the H_w field to provide a "write margin" in excess of H_s.

In practice, the switching characteristic of each memory cell 120 varies among the magnetic memory cells in the array due to manufacturing variations. In addition, the switching characteristic may be such that lower magnitudes of the H_x or H_y fields can cause switching in the magnetic memory cells 20b and

5   20d in the presence of a perpendicular field. This may be due to a variety of factors. For example, there may be manufacturing variations in the crystalline anisotropy value (Hk) of the sense layers of the magnetic memory cells. In addition, there may be variations in the thickness or shape of the magnetic layers of the magnetic memory cells. For example, photolithography process steps may

10   produce rounded edges rather than rectangular edges on the data storage layers. Moreover, data storage layers having square rather than rectangular shapes may have significantly different switching characteristics.

The problems produced in MRAM devices by the presence of stray or external magnetic fields can be appreciated by recognizing that the orientation of

15   magnetization of sense layer 122 may be switched when the total magnetic field to which the memory cell is subjected exceeds H_s. In some instances, stray magnetic fields may have a magnitude sufficient to switch the logic state of a memory cell when combined only with H_x or H_y. A stray magnetic field could also exceed H_s on its own and switch the logic state of a memory cell in the

20   complete absence of a write field H_x or H_y.

The problems caused by stray magnetic fields increase as memory cells are made smaller and are more densely packed into an array of memory cells and associated write conductors (referred to herein as a memory array). Each individual memory cell is subject to greater influence by the magnetic fields of

25   adjacent memory cells and their associated write conductors. The possibility that a stray magnetic field may cause the total magnetic field of an individual memory cell to exceed H_s increases. Thus, reducing or eliminating the effects of stray magnetic fields becomes increasingly important as memory cells shrink in size and the storage densities of memory arrays increase.

30   In the present invention, the effect of stray magnetic fields is reduced or eliminated by positioning a permeable metal shield layer in close proximity to

the memory cells, either individually or in a memory array, to shield the memory cells from the stray fields. Magnetic flux lines, like electrical currents, will always follow the path of least resistance. In magnetic terms, this means that flux lines will follow the path of greatest permeance (lowest reluctance). So

5   long as the material through which the flux is passing does not reach its saturation level, the material will substantially contain the flux lines passing through it. In this manner, a stray magnetic field is prevented from reaching and interfering with the switching of a memory cell in a memory array.

Figure 4 schematically illustrates one embodiment of the invention in

10   which a memory cell 120, having sense layer 122, reference layer 124, tunnel barrier 126 and write lines 130, 132 is shielded by magnetically permeable (or simply "permeable") metal shield layer 140. Because permeable metal shield layer 140 is metallic, it is also electrically conductive and is separated from write lines 130, 132 by an electrically insulating layer 142. Insulating layer 142 may

15   be formed of, for example, SiO_2, tantalum, or any other suitable electrically insulating material. A passivation or capping layer 144, formed of a material like that used for insulating layer 142, may optionally be provided over permeable metal shield layer 140.

To maximize the effectiveness of permeable metal shield layer 140

20   against stray magnetic fields, shield layer 140 should be positioned as close as possible to memory cell 120. In one embodiment, the thicknesses of write conductors 130, 132 and insulating layer 142 are such that permeable metal layer 140 is spaced from memory cell 120 by a distance of less than 10 microns. However, permeable metal shield layer 140 may be positioned at greater

25   distances and still be effective. Although permeable metal shield layer 140 and insulating layer 142 are shown in Figure 4 adjacent sense layer 122 and write line 132, layers 140, 142 could also be positioned adjacent the opposite side of memory cell 120, or on both sides of memory cell 120. This is true for all embodiments of the invention shown and discussed herein.

30   Although Figure 4 illustrates only a single memory cell 120, it is anticipated that a plurality of memory cells 120 will be formed into a memory

array, and permeable metal shield layer 140 will extend over the entire memory array in a manner consistent with that illustrated in Figure 4.

As noted above, so long as permeable metal shield layer 140 through which the flux is passing does not reach its saturation level, the shield layer 140

5   will substantially contain the flux lines passing through it. The saturation level of the permeable metal shield layer 140 may be increased by increasing the size of the shield layer (area and thickness) relative to the size of the memory cell or array, and/or by using a material having a higher permeability to form shield layer 140. For example, where the size of permeable metal shield layer 140 is

10   close to that of the memory array, it is desirable that permeable metal shield layer 140 is formed from a material having a permeability higher than that of the magnetic layers of memory cells 120. If the size of permeable metal shield layer 140 is much greater than that of the memory array, the permeable metal shield layer 140 may be formed from a material having a permeability closer to the

15   permeability of the magnetic layers of memory cells 120.

In one embodiment schematically illustrated in Figures 5a and 5b, a magnetic memory array 150 is positioned within a package 152 which provides the electronics and input/output means for controlling operation of the memory array 150. Memory array 150 may include multiple layers of memory cells and

20   associated write lines. In alternate embodiments of the invention, each layer of memory cells may have its own associated shield layer 140. The package may, for example, have a length and width which are each more than twice those of memory array 150. It is thus possible to extend the permeable metal shield layer 140 (and insulating layer 142) over substantially the entire area of package 152.

25   Memory array 150 would then be provided with shield layers 140 having an area over four times larger than the area of memory array 150.

In one embodiment of the invention, permeable metal shield layer 140 is a soft magnetic material having high permeability (μ) and low anisotropy (Hk). As known to those skilled in the art, soft magnetic materials are those which

30   exhibit magnetic properties only when they are subject to a magnetizing force, such as the magnetic field created when current is passed through wire

surrounding a soft magnetic core. Because the orientation of a stray magnetic field will typically not be known, and in fact may vary from source to source, it may also be desirable to form the permeable metal shield layer from an isotropic material. In this manner, the effect of stray magnetic fields having any

5   orientation may be addressed.

The permeable metal shield layer may be formed of, for example, an alloy of Ni, Fe, and/or Co, or Co alone. Those skilled in the art will recognize other suitable metals and alloys which may be used as well. In one embodiment of the invention, when the size of the permeable metal shield layer is sufficiently

10   greater than the size of the memory array, the material may have a permeability as low as 10. In another embodiment of the invention, when the size of permeable metal shield layer is sufficiently greater than the size of the memory array, the permeable metal shield layer may have an anisotropy as high as 100 Oe.

15   Permeable metal layer 140 may be attached on insulating layer 142 in any suitable manner known in the art. Examples of methods which may be used to attach metal layer 140 include sputtering and spin coating. The permeable metal layer 140 can be made isotropic by, for example, depositing it in the presence of a rotating magnetic field, or by annealing the permeable metal layer

20   140 in the presence of a rotating magnetic field. Annealing the previously deposited permeable metal layer 140 in the presence of a rotating magnetic field may be accomplished by either rotating the assembly having layer 140 in a uniform stationary field, or rotating the magnetic field itself (such as by rotating a permanent magnet) in the annealing station. The annealing temperature of

25   permeable metal layer 140 is preferably lower than the annealing temperature of the magnetic materials used in memory cell 120. This is done to avoid altering the magnetic orientation of magnetic layers 122, 124 while annealing permeable metal shield layer 140.

In another embodiment of the invention, permeable metal layer 140 is a

30   separate layer which is attached to a completed MRAM module or package. For example, as schematically illustrated in Figure 6, a memory array 150' is

constructed as part of a package 152' which provides the electronics and input/output means for controlling operation of the memory array 150'. Memory array 150' may include multiple layers of memory cells and associated write lines, as with memory array 150 above. However, unlike memory array 150, in

5   memory array 150' each layer of memory cells does not have its own associated shield layer 140. Rather, after package 152' is constructed, a permeable metal layer 140' is secured to one or more surfaces of package 152'. Permeable metal layer 140' may, for example, be a thin foil of high permeability material, such a Mumetal ® or Permalloy® which is secured to package 152' by a suitable

10   adhesive. The material of insulating layer 142' may itself be an adhesive material used to secure permeable metal layer 140' to package 152'.

The thicknesses of the memory array 150' and package 152' are very small compared to their length and width (Figures 5a and 6 show greatly exaggerated thicknesses), and the thickness of permeable metal layer 140' is

15   large compared to the thickness of memory array 150' (by several orders of magnitude). Thus, permeable metal layer 140' may be secured to the surface of package 152' and still provide suitable shielding from stray magnetic fields.

Although specific embodiments have been illustrated and described herein for purposes of description of the preferred embodiment, it will be

20   appreciated by those of ordinary skill in the art that a wide variety of alternate and/or equivalent implementations calculated to achieve the same purposes may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. Those with skill in the mechanical, electro-mechanical, electrical and chemical arts will readily

25   appreciate that the present invention may be implemented in a very wide variety of embodiments. This application is intended to cover any adaptations or variations of the preferred embodiments discussed herein. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents and thereof.

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